

Remarks/Arguments

35 U.S.C. §103

Claims 1, 3-7, and 10, stand rejected under 35 U.S.C. §103(a) as being unpatentable over Valmiki et al. (U.S. Patent No. 6,636,222, hereinafter referred to as “Valmiki”), in view of Terao et al. (U.S. Patent Publication No. 2001/0055011, hereinafter referred to as “Terao”).

Independent claims 1 and 10 have been amended to clarify that the second graphics object is converted into “still” picture data.

It is respectfully asserted that neither Valmiki nor Terao, alone or in combination, disclose:

“means for converting the second graphics object into still picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated,”

as described in currently amended claim 1. Furthermore, the combination of Valmiki and Terao would not permit the display two graphics objects under the described OSD limitations as would the teaching of claim 1.

Among the problems addressed by the present invention are the limitations of certain OSD processors, in particular the limitation that certain OSD processors cannot display two graphic objects that overlap, or in some cases, share the same lines of the screen. To address this problem, the present application discloses an apparatus that converts the second of two overlapped graphics into a stationary picture memory separate from the OSD path, which in turn is combined by a mixer with the OSD plane containing the first graphic. The end result is the display of the two overlapping graphics, despite the inability of the OSD processor to perform such display on its own.

In contrast, Valmiki is not concerned with working around the limitations of OSD processors, but instead with rendering compressed video data within an allotted number of clock cycles. More specifically, Valmiki teaches a system where “a video and graphics system processes video data including both analog video, e.g., NTSC/PAL/SECAM/S-video, and digital video, e.g., MPEG-2 video in SDTV or HDTV format. The video and graphics system includes a video decoder, which is capable of concurrently decoding multiple SLICES of MPEG-2 video data. The video decoder includes multiple row decoding engines for decoding the MPEG-2 video data. Each row decoding engine concurrently decodes two or more rows of the MPEG-2 video data. The row decoding engines have a pipelined architecture for concurrently decoding multiple rows of MPEG-2 video data. The video decoder may be integrated on an integrated circuit chip with other video and graphics system components such as transport processors for receiving one or more compressed data streams and for extracting video data, and a video compositor for blending processed video data with graphics.” (Valmiki Abstract)

Valmiki discloses that its “video decoder includes multiple row decoding engines,” but does not describe detection of overlaps or movement of an object from an OSD plane to a picture plane in response. As such, Valmiki does not disclose means for converting a second graphics object into still picture data if an overlap is detected between first and second graphics objects. Thus, it is respectfully submitted that Valmiki fails to disclose “means for converting the second graphics object into a still picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated,” as described in currently amended claim 1.

Terao teaches an invention whose goal is “to provide an information processor which, in case a component in which a moving picture is displayed is overlapped by another window, can apply display effect only to a region on which the moving picture is actually displayed.” (Terao Abstract) Terao deals with improving an image displayed on a CRT display (Terao [0002] to [0004]), but applies that improvement only to the region of the moving picture that is displayed. (Terao [0007] and [0008])

The method of Terao comprises the steps of detecting overlapping windows, identifying the region of the moving picture that is not overlapped, and applying the image improvement to that region only. Terao does disclose means for detecting an overlap between a first graphics object (the moving picture) and a second graphics object. (Terao, [0056] to [0059]) However, Terao does not disclose means for converting the first graphics object into still picture data if the overlap cue is generated. Instead, Terao indicates that the image improvement process is applied only to the visible region of the moving picture. (Terao, [0069] to [0091]) That moving picture is not converted into still picture data. Therefore, Terao, like Valmiki, fails to disclose “means for converting the second graphics object into a still picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated,” as described in currently amended claim 1.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Valmiki or Terao, alone or in combination, that makes the present invention as claimed in currently amended claim 1 unpatentable. It is also respectfully submitted that independent claim 10 is allowable for at least the same reasons as currently amended claim 1. Since dependent claims 3-7 are dependent from allowable independent claim 1, it is submitted that they too are allowable for at least the same reasons claim 1 is allowable. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's representative at (609) 734-6804, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

/Brian J. Cromarty/

By: Brian J. Cromarty
Reg. No. 64018
Phone (609) 734-6804

Patent Operations
Thomson Licensing Inc.
P.O. Box 5312
Princeton, New Jersey 08543-5312
April 28, 2009